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THIN FILM TRANSISTOR
[HAKUMAKU TORANJISUTA]

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Specifications

1. Title of the Invention

Thin Film Transistor

2. Claim(s)

1. In a MOS-type thin film semiconductor element having a source and drain region with a first conductive type in a polycrystalline semiconductor layer formed on an insulating substrate and having a gate electrode between these regions by way of a gate insulation film, a thin film transistor characterized by the gate insulating film coming in contact with the insulating substrate within a region surrounded by the semiconductor interface, source and drain joint faces and insulating substrate, and having a defect layer containing defects serving as the recombination center of a carrier only in a region separated a prescribed distance from the gate insulating film/semiconductor interface and the source and drain joint faces at or above the defect concentration in the parent semiconductor.

2. The thin film transistor of Claim 1 characterized by making the distance from the gate insulating film-semiconductor interface and the source and drain joint faces to the defect layer being at least 1,000Å.

3. The thin film transistor of claim 1 characterized by the density of the defects contained in the defect layer in the vicinity of the Fermi level being at least 1×10^{18} cm^{-3} eV^{-1}.

3. Detailed Specifications

(Field of Industrial Application)

The present invention pertains to a semiconductor thin film element formed on an insulating substrate, and in particular, it relates to a

thin film transistor having ideal characteristics for use in driving a liquid crystal display panel.

(Prior Art)

Technical developments in forming thin film active elements are being performed proactively with amorphous and polycrystalline semiconductors on insulating substrates. An application in such technology is a thin film transistor active [misspelled in source as 'mactive'] matrix for driving a liquid crystal display panel (the thin film transistor is called "TFT" below). Using the TFT active matrix for driving the liquid crystal in the liquid crystal display panel under an intense light irradiation of 10^3 lx to 10^4 lx is unavoidable from the standpoint of the device structure thereof. But when a TFT is driven under this intense exposure to light, the off-current increases due to the photoexcited carrier in the channel region, which greatly hinders this TFT from driving the liquid crystal. Effective methods in which the thickness of a semiconductor thin film is reduced are discussed in Tokkai Nos. 61-85868 and 61-65476.

(Problems to be Solved by the Invention)

However, a coplanar TFT in which the drain and source regions are formed in a self-aligning manner had problems if the thickness of the semiconductor film was reduced because (1) the resistances of the source and drain regions increased, (2) the process conditions were severe during gate patterning and (3) a high-quality semiconductor film was not obtained.

The present invention solves these problems and the object thereof is to obtain a TFT with a structure having characteristics wherein the off-current is as small as if the semiconductor film is rendered thin

but without reducing the thickness thereof.

(Means for Solving the Problems)

The present invention is characterized by suppressing the generation of a photoelectric current within this region and controlling an increase in the off-current during light irradiation by producing defects at a density of at least 10^{18} cm^{-3} eV^{-1} by ion implantation in a specified region in the TET channel region, and furthermore, preventing an increase in the leakage current in the reverse direction by generating defects by avoiding the space-charge regions formed in the vicinities of the source and drain regions.

(Operation)

The structure of the TFT of the present invention is shown in Figure 1. The thicknesses of the effective channel regions are reduced from t_1 to t_2 due to the presence of a high-resistance highly concentrated defect layer **10** and the off-current is reduced in the same way as when the thickness is reduced. Furthermore, the surplus carrier is photoexcited in the channel regions during light irradiation. A relation is established between the life τ of the surplus carrier and the density N_t of the recombination center:

$\tau=1/N_t$.

Hence, the life of the surplus carrier generated in the highly concentrated defect layer **10** is shortened and it is immediately recombined and hardly contributes to conduction at all. Furthermore, the carriers generated in channel regions having few defects between the defect layer **10** and the gate insulating film **2** are dispersed in the direction of the defect

layer 10 due to the concentration distribution of the carriers produced in the perpendicular direction; hence, the effects on reducing the off-current is much more effective than reducing the film thickness from t_1 to t_2.

Next, the action of the offset of the length L_D between the drain and source junction faces J_1 and J_2 and the defect layer 10 is explained through Figure 3.

Space-charge layers 20 are formed in the vicinities of the drain and source junctions J_1 and J_2, but when defects exist so as to become the recombination center within these regions, the leakage current increases in the reverse direction when the gate voltage is negative. Figure 4 is a drawing comparing a TFT having different defect densities within the channel regions with the TFT having a conventional structure shown in Fig. 3, but it is seen that the off characteristic i decreases in the reverse direction in order of A→B→C as the defect density increases.

If the defects exist so as to form levels in the forbidden bands in the space-charge regions having intense electric fields, an extremely large leakage current is conducted due to tunneling through these defects or the generation of carriers. The fine mechanisms of this leakage current is still not clear enough, but if the number of defects within the space-charge regions is high, it is seen that the leakage current increases. Therefore, as in the present invention, it is extremely important to prevent deterioration of the leak characteristic in the reverse direction by providing an offset between the junction faces and the defect layer and not introducing defects into the space-charge layer.

This offset length L_D is determined by the local level density N_L in the vicinity of the Fermi level within the polycrystalline or amorphous silicon film which is the parent material. For example, when the local level density N_L in the vicinity of the Fermi level is about 10^{18} cm^{-3} eV^{-1}, the space-charge region width is about 1,000Å. If the spread of the space-charge layer and the mask aligning accuracy are considered when a reverse bias is applied, the offset length L_D should be 5 to 10 μm.

(Practical Examples)

The manufacturing steps in the practical example of the present invention shown in Fig. 1 will now be explained through Fig. 2. A polycrystalline silicon film is deposited to 1,500Å, for example, on the insulating substrate **1** by reduced-pressure CVD, and the same is patterned to obtain an island-shaped element region **8**. Next, the resist **11** is formed, as shown in Fig. 2(B), Ar^+ ions, for example, are implanted by ion implantation at conditions including an acceleration voltage of 110 KeV and a dosage of 1×10^{16} cm^{-2} after masking this resist. Continuing, the resist is removed, after which an SiO_2 film is deposited by normal pressure CVD, and in succession, a polycrystalline silicon film is deposited by reduced-pressure CVD, and the same is patterned to form the gate insulating film **2** and the gate electrode **3**, as shown in Fig. 2(C). p^+ ions, for example, are implanted next, as shown in Fig. 2(D), to form the drain region **5** and source region **6**. Continuing, a lamellar insulating film is formed by normal pressure CVD, as shown in Fig. 2(E), to form a contact hole. Finally, a contact electrode **7** is formed by vapor depositing Al and patterning it, and a TFT is obtained with the structure shown in Fig. 1.

In this practical example, the case of a polycrystalline silicon was explained as an example, but when amorphous silicon is used, the present invention can be applied in the same manner. The implanted ions are not limited to Ar^+ ions in order to generate a high concentration of defects; they can be any electrically active ions which do not become donors or acceptors in the silicon. For example, they may be O^+, N^+ ions and the like.

(Advantages of the Invention)

There are advantages according to the present invention wherein the semiconductor film thickness is reduced, the leakage characteristics in the reverse direction do not deteriorate, and the off-current can be reduced equal to or better than by making a thin film during light irradiation.

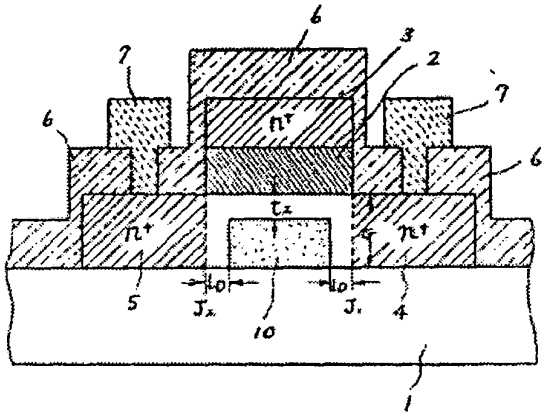
4. Brief Explanation of the Drawings

Figure 1 is a sectional schematic diagram of a practical example of the present invention; Figures 2(A) to (F) are process drawings showing a method of manufacture of the practical example in Fig. 1; Figure 3 is a sectional schematic drawing of the TFT with a conventional structure; Figure 4 is a drawing showing the dependency of the off characteristics of a TFT having the structure in Fig. 3 on the defect density of the silicon film.

1: insulating substrate; 2: gate insulating film; 3: gate electrode; 4: n^+ drain region; 5: n^+ source region; 6: source region; 7: contact electrode; 8: i channel region; 9: polycrystalline silicon layer; 10: high concentration defect layer; J_1: drain junction; J_2: source junction; t_1: polycrystalline silicon film thickness; t_2: distance between defect layer 10 and gate

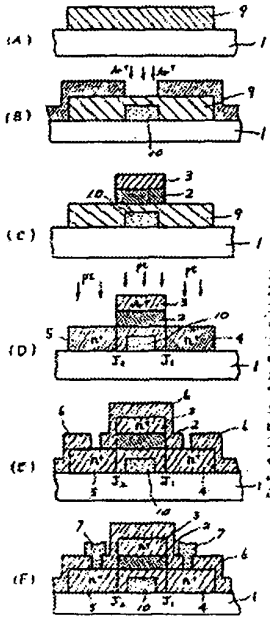
insulating film; L_D: distance between defect layer 10 and drain region 4 and source region 5

Figure 1



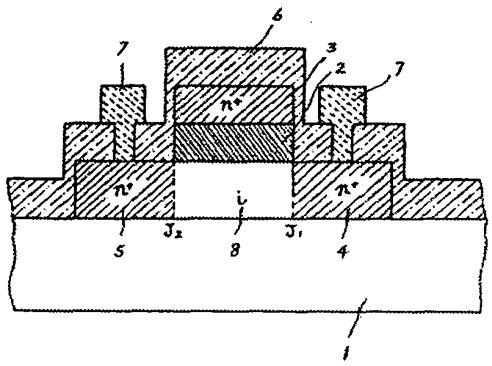
1: insulating substrate
2: gate insulating film
3: gate electrode
4: n+ drain region
5: n+ source region
6: lamellar insulating film
7: contact electrode
10: highly concentrated defect layer
J1: drain junction
J2: source junction
t2: distance between defect layer and gate insulating film
LD: distance between defect layer and source and drain regions

Figure 2



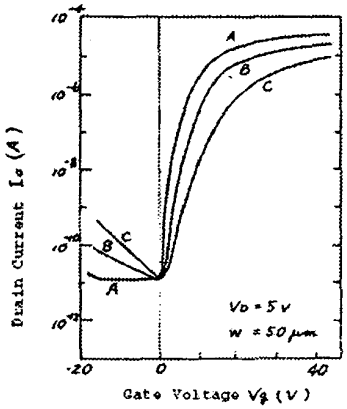
1: insulating substrate
2: gate insulating film
3: gate electrode
4: n+ drain region
5: n+ source region
6: lamellar insulating film
7: contact electrode
9: polycrystalline silicon film
10: highly concentrated defect layer
J1: drain junction
J2: source junction

Figure 3



1: insulating substrate
2: gate insulating film
3: gate electrode
4: n+ drain region
5: n+ source region
6: lamellar insulating film
7: contact electrode
J1: drain junction
J2: source junction

Figure 4



A : $N_L = 5 \times 10^{19}\ cm^{-3}\ eV^{-1}$

B : $N_L = 2 \times 10^{18}\ cm^{-3}\ eV^{-1}$

C : $N_L = 5 \times 10^{18}\ cm^{-3}\ eV^{-1}$

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1,3-11 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Konishi '573.

The previous rejection still applies. The new limitations do not structurally distinguish over Konishi because figure 1 of Konishi shows the recombination centers being separated from the drain region by a distance Lo which appears to be somewhere between 1/3 to 1/10 of the channel length. New claim 11 is rejected because the recited thickness is typical for a short channel thin film device as Konishi and the recombination centers in Konishi do not span the entire channel length. If applicant's can prove that the distance Lo in Konishi is not within the claimed range, claims 1-11 will be allowed.

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 recites a volumetric center of the recombination centers being 1/3 to 1/10 of the channel length from the drain. Konishi shows the volumetric center being at the halfway point.

Applicant's arguments filed 1/7/02 have been fully considered but they are not persuasive. Applicant's state that Konishi does not teach recombination centers at the claimed distance. However, as stated above, the figures of Konishi show the recombination centers to be located at the proper distance from the drain, as claimed. The Konishi article is being translated by the Patent Office.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,4-10 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Nakaoka '500.

Nakaoka teaches a recombination region in the channel near the drain region. Claims 1,2,4-7,9,10 are anticipated or obvious over '500. Claim 8 is obvious because it would have been routine experimentation to place the recombination centers at the locations of most efficacious performance. A location near the gate electrode would not appear to be as useful as near the bottom of the channel because it would quench

useful channel current. Nevertheless it is considered obvious to one of ordinary skill and not producing any unexpected useful results.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Konishi '573.

Konishi teaches a recombination region in the channel near the drain region. Claims 1-10 are anticipated or obvious over '573. Note in regard to claim 8 that the recombination region 10 is also located near the side of the gate electrode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Jackson Jr. whose telephone number is 703 308 4937. The examiner can normally be reached on t-th 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lee can be reached on 703 308 4915. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7722 for regular communications and 703 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

jj
September 6, 2002

JEROME JACKSON
PRIMARY EXAMINER